

FORM PTO-1449 SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT			ATTY. DOCKET NO. 1778.1730000	APPLICATION NO. 09/702,112	
			FIRST NAMED INVENTOR Michael Gottlieb Jensen		
			FILING DATE October 30, 2000		

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB- CLASS	FILING DATE
RLE	AA1	3,794,980	02/1974	Cogar <i>et al.</i>	—	—	—
RLE	AB1	3,811,114	05/1974	Lemay <i>et al.</i>	—	—	—
RLE	AC1	3,840,861	10/1974	Amdahl <i>et al.</i>	—	—	—
RLE	AD1	3,983,541	09/1976	Faber <i>et al.</i>	—	—	—
RLE	AE1	4,110,822	08/1978	Porter <i>et al.</i>	—	—	—
RLE	AF1	4,149,244	04/1979	Anderson <i>et al.</i>	—	—	—
RLE	AG1	4,229,790	10/1980	Gilliland <i>et al.</i>	—	—	—
RLE	AH1	4,295,193	10/1981	Pomerene, James H.	—	—	—
RLE	AI1	4,432,056	02/1984	Aimura, Harutsugu	—	—	—
RLE	AJ1	4,467,409	08/1984	Potash <i>et al.</i>	—	—	—

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB- CLASS	TRANSLATION
RLE	AK1	EP 0 073 424 A2	03/1983	Europe EPO	—	—	N/A
RLE	AL1	EP 0 239 081 B1	09/1995	Europe EPO	—	—	N/A
RLE	AM1	EP 0 368 332 B1	09/1997	Europe EPO	—	—	N/A

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

RLE	AN1	U.S. Utility Patent Application No. 09/702,115, inventors Jensen, M., <i>et al.</i> , filed October 30, 2000 (not published) (71 pages).
RLE	AO1	U.S. Reissue Patent Application No. 10/066,475, inventor Edward Colles Nevill, filed February 1, 2002 (based on U.S. Pat. No. 6,021,265, issued February 1, 2000) (9 pages).
RLE	AP1	Preliminary Amendment, filed February 1, 2002, in U.S. Reissue Patent Application No. 10/066,475, inventor Edward Colles Nevill, filed February 1, 2002 (based on U.S. Pat. No. 6,021,265, issued February 1, 2000) (15 pages).
RLE	AQ1	Case, Brian, "ARM Architecture Offers High Code Density: Non-traditional RISC Encodes Many Options in Each Instruction," <i>Microprocessor Report</i> , Vol. 5, No. 23, pgs. 11-14 (December 18, 1991).
RLE	AR1	Cobb, Paul, "TinyRISC: a MIPS-16 embedded CPU core," Presentation for Microprocessor Forum, 13 slides (7 pages) (October 22-23, 1996).

EXAMINER <i>Richard Ellis</i>	DATE CONSIDERED <i>9/26/2005</i>
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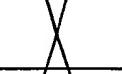
U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
RUE	AA2	4,507,728	03/1985	Sakamoto <i>et al.</i>	—	—	—
RUE	AB2	4,685,080	08/1987	Rhodes, Jr. <i>et al.</i>	—	—	—
RUE	AC2	4,724,517	02/1988	May, Michael D.	—	—	—
RUE	AD2	4,777,594	10/1988	Jones <i>et al.</i>	—	—	—
RUE	AE2	4,782,441	11/1988	Inagami <i>et al.</i>	—	—	—
RUE	AF2	5,132,898	07/1992	Sakamura <i>et al.</i>	—	—	—
RUE	AG2	5,241,636	08/1993	Kohn, Leslie D.	—	—	—
RUE	AH2	5,355,460	10/1994	Eickemeyer <i>et al.</i>	—	—	—
RUE	AI2	5,463,700	10/1995	Nakazawa, Tamotsu	—	—	—
RUE	AJ2	5,467,134	11/1995	Laney <i>et al.</i>	—	—	—
FOREIGN PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
RUE	AK2	EP 0 449 661 B1	11/1995	Europe EPO	—	—	N/A
 	AL2						Yes No
 	AM2						Yes No
OTHER (Including Author, Title, Date, Pertinent Pages, etc.)							
RUE	AN2	Gwennap, Linley, "VLIW: The Wave of the Future?: Processor Design Style Could Be Faster, Cheaper Than RISC," <i>Microprocessor Report</i> , Vol. 8, No. 2, pp. 18-21 (February 14, 1994).					
RUE	AO2	Kurosawa, K., et al., "Instruction Architecture For A High Performance Integrated Prolog Processor IPP," <i>Logic Programming: Proceedings of the Fifth International Conference and Symposium (August 15-19, 1988)</i> , MIT Press, Cambridge, MA, Vol. 2, pp. 1506-1530 (1988).					
RUE	AP2	LSI TinyRisc Development (visited April 24, 2001), at < http://www.redhat.com/support/manuals/gnupro99rl/6_embed/emb09.html >, 13 pages.					
RUE	AQ2	NEC Data Sheet, MOS Integrated Circuit, uPD30121, VR4121 64-/32-Bit Microprocessor (Copyright NEC Electronics Corporation 2000) (76 pages).					
RUE	AR2	NEC User's Manual, VR4100 Series™, 64-/32-Bit Microprocessor Architecture, pp. 1-11 and 54-83 (Chapter 3) (Copyright NEC Corporation 2002).					
EXAMINER <i>Richard Ellis</i>					DATE CONSIDERED <i>0/26/2005</i>		

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U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
RUE	AA3	5,506,974	04/1996	Church <i>et al.</i>	—	—	—
RUE	AB3	5,546,552	08/1996	Coon <i>et al.</i>	—	—	—
RUE	AC3	5,574,873	11/1996	Davidian, Gary G.	—	—	—
RUE	AD3	5,577,200	11/1996	Abramson <i>et al.</i>	—	—	—
RUE	AE3	5,619,666	04/1997	Coon <i>et al.</i>	—	—	—
RUE	AF3	5,732,234	03/1998	Vassiliadis <i>et al.</i>	—	—	—
RUE	AG3	5,751,932	05/1998	Horst <i>et al.</i>	—	—	—
RUE	AH3	5,794,010	08/1998	Worrell <i>et al.</i>	—	—	—
RUE	AI3	5,896,519	04/1999	Worrell, Frank	—	—	—
RUE	AJ3	5,948,112	09/1999	Shimada <i>et al.</i>	—	—	—
FOREIGN PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
X	AK3						Yes No
X	AL3						Yes No
X	AM3						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN3	Ross, Roger, "There's no risk in the future for RISC," <i>Computer Design</i> , Vol. 28, No. 22, pp. 73-75 (November 13, 1989).
	AO3	
	AP3	
	AQ3	
	AR3	

EXAMINER	Richard E. Ells	DATE CONSIDERED	01/26/2005
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<i>RUE</i>	AA4	5,982,459	11/1999	Fandrianto <i>et al.</i>	—	—	—
<i>RUE</i>	AB4	6,266,765 B1	07/2001	Horst, Robert W.	—	—	07/07/2000
<i>RUE</i>	AC4	6,272,620 B1	08/2001	Kawasaki <i>et al.</i>	—	—	04/04/2000
<i>RUE</i>	AD4	2001/0021970 A1	09/2001	Hotta <i>et al.</i>	—	—	05/14/2001
<i>RUE</i>	AE4	2004/0054872 A1	03/2004	Nguyen <i>et al.</i>	—	—	09/12/2003
	AF4						
	AG4						
	AH4						
	AI4						
	AJ4						

FOREIGN PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
		AK4					Yes No
		AL4					Yes No
		AM4					Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)							
	AN4						
	AO4						
	AP4						
	AQ4						
	AR4						

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